What is claimed:

1. A semiconductor device comprising:

an insulation layer;

a semiconductor layer formed on the insulation layer;

an element isolation region formed in the semiconductor layer; and

a first element forming region and a second element forming region defined by the element isolation region;

wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor;

the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type,

the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type,

the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type,

the first body region of the second conduction type is electrically connected to the source region of the first conduction type,

the first body region of the second conduction type is electrically connected to the first base region of the second conduction type,

the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and

the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and

wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor.

the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type,

the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer.

2. A semiconductor device according to claim 1, further comprising:

a first electrode layer that continues to a side section of the first gate electrode layer and reaches the element isolation region,

wherein the first gate electrode layer is formed in a manner to cross over the element forming region,

the source region of the first conduction type is formed in a first region surrounded by the first gate electrode layer in a forming region of the first field effect transistor, the first electrode layer, and the element isolation region,

the drain region of the first conduction type and the collector region of the first conduction type are formed in a second region surrounded by the first gate electrode layer and the element isolation region,

the emitter region of the first conduction type is formed in a third region surrounded by the first gate electrode layer in a forming region of the first bi-polar transistor, the first electrode layer and the element isolation region, and

the first body region of the second conduction type is formed at least below the first gate electrode layer in the forming region of the first field effect transistor, and below a part of the first electrode layer.

3. A semiconductor device according to claim 2, further comprising:

a second electrode layer having one end section that continues to a side section of the second gate electrode layer and another end section that reaches the element isolation region,

wherein the second gate electrode layer is formed in a manner to cross over the second element forming region,

the drain region of the second conduction type is formed in a fourth region surrounded by the second gate electrode layer in the forming region of the second field effect transistor, the second electrode layer, and the element isolation region,

the source region of the second conduction type and the collector region of the first conduction type are formed in a fifth region surrounded by the second gate electrode layer and the element isolation region,

the emitter region of the first conduction type is formed in a sixth region surrounded by the second gate electrode layer in the forming region of the second bi-polar transistor, the second electrode layer and the element isolation region, and

the first body region of the first conduction type is formed below the second gate electrode layer.

4. A semiconductor device according to claim 1, further comprising:

a first layer and a second layer, wherein

the first layer has one end section continuing to the first gate electrode layer or the second layer, and another end section reaching the element isolation region,

the second layer has one end section continuing to the first gate electrode layer or the second layer, and another end section reaching the element isolation region,

the source region of the first conduction type is formed in a first region surrounded by the first gate electrode layer, the first layer and the element isolation region,

the drain region of the first conduction type and the first collector region of the first conduction type are formed in a second region surrounded by the first gate electrode layer, the second layer and the element isolation region,

the first emitter region of the first conduction type is formed in a third region surrounded by the first layer, the second layer and the element isolation region,

the first base region of the second conduction type is formed below a part of the first layer, and below a part of the second layer in the semiconductor layer, and

the first body region of the second conduction type is formed at least below the first gate electrode layer and below a part of the first layer in the semiconductor layer.

5. A semiconductor device according to claim 4, further comprising:

a third layer and a fourth layer, wherein

the third layer has one end section continuing to the second gate electrode layer or the fourth layer, and another end section reaching the element isolation region,

the fourth layer has one end section continuing to the second gate electrode layer or the third layer, and another end section reaching the element isolation region,

the drain region of the second conduction type is formed in a fourth region surrounded by the second gate electrode layer, the third layer and the element isolation region,

the source region of the second conduction type and the second collector region of the first conduction type are formed in a fifth region surrounded by the second gate electrode layer, the fourth layer and the element isolation region,

the second emitter region of the first conduction type is formed in a sixth region surrounded by the third layer, the fourth layer and the element isolation region,

the second base region of the second conduction type is formed below a part of the third layer and below a part of the fourth layer in the semiconductor layer, and

the first body region of the first conduction type is formed at least below the second gate electrode layer and below a part of the fourth layer in the semiconductor layer, and

a second body region of the second conduction type is provided in the semiconductor layer below a part of the third layer for electrically connecting the second body region of the second conduction type and the drain region of the second conduction type.

6. A semiconductor device according to claim 1, further comprising, in the first element forming region, a second body region of the first conduction type, which is formed in the semiconductor layer between the first base region of the second conduction type and the first collector region of the first conduction type.

7. A semiconductor device according to claim 1, wherein an impurity diffusion layer of the second conduction type is further formed in the first element forming region,

wherein the impurity diffusion layer of the second conduction type is a semiconductor layer in the first region, and is formed in the semiconductor layer between the source region of the first conduction type and the first body region of the second conduction type, and

the source region of the first conduction type and the first body region of the second conduction type are electrically connected to one another through the impurity diffusion layer of the second conduction type.

8. A semiconductor device according to claim 7, wherein a contact layer for electrically connecting the impurity diffusion layer of the second conduction type and the source region of the first conduction type is formed, wherein the contact layer is formed in a manner to cross over the impurity diffusion layer of the second conduction type and the source region of the first conduction type.

9. A semiconductor device according to claim 1, wherein a third body region of the second conduction type is formed in the semiconductor layer between the first collector region of the first conduction type and the first emitter region of the first conduction type and in the semiconductor layer adjacent to the element isolation region.

10. A semiconductor device according to any one of claim 8, wherein a contact layer for electrically connecting the source region of the second conduction type and the second contact region of the first conduction type is formed in the second element isolation region, wherein the contact layer is formed in a manner to cross over the source region of the second conduction type and the second collector region of the first conduction type.

11. A semiconductor device according to any one of claim 9, wherein a fourth body region of the second conduction type is formed in the semiconductor layer between the second collector region of the first conduction type and the second emitter region of the first conduction type, and in the semiconductor layer adjacent to the element isolation region.

12. A semiconductor device according to claim 1, wherein the first conduction type is n-type, and the second conduction type is p-type.

13. A semiconductor device according to claim 1, wherein the first conduction type is p-type, and the second conduction type is n-type.

14. A semiconductor device according to claim 1, wherein the semiconductor layer is a silicon layer.

15. A semiconductor device comprising:

an insulation layer;

a semiconductor layer formed on the insulation layer;

an element isolation region formed in the semiconductor layer; and

a first element forming region and a second element forming region defined by the element isolation region,

wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor,

a first gate electrode layer is formed on the semiconductor layer,

the first gate electrode layer is formed in a manner to cross over the first element forming region,

a first electrode layer is formed on the semiconductor layer,

the first electrode layer has one end section continuing to a side section of the first gate electrode layer, and another end section reaching the element isolation region,

a first impurity diffusion layer of a first conduction type is formed at least in a part of a first region surrounded by the first gate electrode layer in a forming region of the first field effect transistor, the first electrode layer and the element isolation region,

a second impurity diffusion layer of the first conduction type is formed in a second region surrounded by the first gate electrode layer and the element isolation region,

a third impurity diffusion layer of the first conduction type is formed in a third region defined by the first gate electrode layer in a forming region of the first bi-polar transistor, the first electrode layer and the element isolation region,

a first body region of a second conduction type is formed below the first gate electrode layer in a forming region of the first field effect transistor and the first electrode layer,

a first impurity diffusion layer of the second conduction type is formed below the first gate electrode layer in the forming region of the first bi-polar transistor and the first electrode layer and along a periphery of the third impurity diffusion layer of the first conduction type,

the first body region of the second conduction type is electrically connected to the first impurity diffusion layer of the first conduction type, and

the first body region of the second conduction type is electrically connected to the first impurity diffusion layer of the second conduction type,

wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor,

a second gate electrode layer is formed on the semiconductor layer,

the second gate electrode layer is formed in a manner to cross over the second element forming region,

a second electrode layer is formed on the semiconductor layer,

the second electrode layer has one end section continuing to a side section of the second gate electrode layer, and another end section reaching the element isolation region,

a second impurity diffusion layer of the second conduction type is formed in a fourth region surrounded by the second gate electrode layer in a forming region of the second field effect transistor, the first electrode layer and the element isolation region,

a third impurity diffusion layer of the second conduction type is formed in a fifth region surrounded by the second gate electrode layer and the element isolation region and in the forming region of the second field effect transistor,

a fourth impurity diffusion layer of the first conduction type is formed in a fifth region in a forming region of the second bi-polar transistor,

a fifth impurity diffusion layer of the first conduction type is formed in a sixth region surrounded by the second gate electrode layer in the forming region of the second bi-polar transistor and the element isolation region,

a body region of the first conduction type is formed below the second gate electrode layer.

a fourth impurity diffusion layer of the second conduction type is formed below the second gate electrode layer in the forming region of the second bi-polar transistor and the second electrode layer and along a periphery of the fifth impurity diffusion layer of the first conduction type,

the body region of the first conduction type is electrically connected to the fourth impurity diffusion layer of the first conduction type,

the third impurity diffusion layer of the second conduction type is electrically connected to the fourth impurity diffusion layer of the first conduction type,

the second impurity diffusion layer of the second conduction type is electrically connected to the fourth impurity diffusion layer of the second conduction type,

the second impurity diffusion layer of the first conduction type is electrically connected to the fifth impurity diffusion layer of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer.

16. A method for manufacturing a semiconductor device including an insulation layer and a semiconductor layer formed on the insulation layer, the method comprising the steps of:

(A) forming an element isolation region in the semiconductor layer to define a first element forming region and a second element forming region; and

(B) forming a first field effect transistor and a first bi-polar transistor in the first element forming region,

wherein the step (B) comprises the steps of:

(B – 1) forming a first body region of a second conduction type in the semiconductor layer at least in a forming region where a first gate electrode layer is to be formed,

(B – 2) forming a first gate electrode layer and a first electrode layer on the semiconductor layer in the first element forming region, wherein the first electrode layer continues to the first gate electrode layer and reaches the element isolation region,

(B – 3) forming a first impurity diffusion layer of the second conduction type in the semiconductor layer in a third region surrounded by the first gate electrode layer in a forming region of the bi-polar transistor, the first electrode layer and the element isolation region,

(B – 4) conducting a thermal treatment to thermally diffuse the first impurity diffusion layer of the second conduction type to form a first base region of the second conduction type of the first bi-polar transistor below a part of the first gate electrode layer and in the semiconductor layer below the first electrode layer, and to electrically connect the first base region of the second conduction type and the first body region of the second conduction type,

(B – 5) forming a source region of a first conduction type of the first field effect transistor at least in a part of a first region surrounded by a first gate electrode layer in a forming region of the first field effect transistor, the first electrode layer and the element isolation region,

(B – 6) forming a drain region of the first conduction type of the first field effect transistor in a part of a second region surrounded by the first gate electrode layer and the element isolation region,

(B – 7) forming a first collector region of the first conduction type of the first bi-polar transistor in a part of the second region,

(B – 8) forming a first emitter region of the first conduction type of the first bi-polar transistor in the third region, and

(B – 9) electrically connecting the first body region of the second conduction type and the source region of the first conduction type;

the step (C) of forming a second field effect transistor and a second bi-polar transistor in the second element forming region,

wherein the step (C) comprises the steps of:

(C – 1) forming a first body region of the first conduction type in the semiconductor layer at least in a forming region where a second gate electrode layer is to be formed,

(C – 2) forming a second body region of the second conduction type at least in a part of the semiconductor layer in a forming region where a second electrode layer is to be formed,

(C – 3) forming a second gate electrode layer and a second electrode layer on the semiconductor layer in the second element forming region, wherein the second electrode layer has one end section continuing to a side section of the gate electrode layer and another end section reaching the element isolation region,

(C – 4) forming a second impurity diffusion layer of the second conduction type in the semiconductor layer in a sixth region surrounded by the second gate electrode layer in a forming region of the second bi-polar transistor, the second electrode layer and the element isolation region,

(C – 5) conducting a thermal treatment to thermally diffuse the second impurity diffusion layer of the second conduction type to form a second base region of the second conduction type of the second bi-polar transistor below a part of the second gate electrode layer and in the semiconductor layer below the second electrode layer, and to electrically connect the second base region of the second conduction type and the second body region of the second conduction type,

(C – 6) forming a drain region of the second conduction type of the second field effect transistor in a fourth region surrounded by a second gate electrode layer in a forming region of the second field effect transistor, the second electrode layer and the element isolation region, and electrically connecting the drain region of the second conduction type to the second base region of the second conduction type through the second body region of the second conduction type,

(C – 7) forming a source region of the second conduction type of the second field effect transistor in a part of a fifth region surrounded by the second gate electrode layer and the element isolation region,

(C – 8) forming a second collector region of the first conduction type of the second bi-polar transistor in a part of the fifth region, and electrically connecting the second

collector region of the first conduction type to the first body region of the first conduction type,

(C – 9) forming a second emitter region of the first conduction type of the second bi-polar transistor in the sixth region, and

(C – 10) electrically connecting the source region of the second conduction type and the second collector region of the first conduction type;

the step (D) of electrically connecting the first collector region of the first conduction type and the second emitter region of the first conduction type; and

the step (E) of electrically connecting the first gate electrode layer and the second gate electrode layer.

17. A method for manufacturing a semiconductor device including an insulation layer and a semiconductor layer formed on the insulation layer, the method comprising the steps of:

(A) forming an element isolation region in the semiconductor layer to define a first element forming region and a second element forming region; and

(B) forming a first field effect transistor and a first bi-polar transistor in the first element forming region,

wherein the step (B) comprises the steps of:

(B – 1) forming a first body region of a second conduction type in the semiconductor layer at least in a forming region where a first gate electrode layer is to be formed and in a forming region where a first layer is to be formed,

(B – 2) forming a first gate electrode layer on the semiconductor layer in the first element forming region,

(B – 3) forming a first layer on the semiconductor layer in the first element forming region, the first layer having one end section continuing to the first gate electrode layer or a second layer, and another end section reaching the element isolation region,

(B – 4) forming a second layer on the semiconductor layer in the first element forming region, the second layer having one end section continuing to the first gate electrode layer or the first layer, and another end section reaching the element isolation region,

(B – 5) forming a first impurity diffusion layer of the second conduction type in the semiconductor layer in a third region surrounded by the first layer, the second layer and the element isolation region,

(B – 6) conducting a thermal treatment to thermally diffuse the first impurity diffusion layer of the second conduction type to form a first base region of the second conduction type of the first bi-polar transistor below a part of the first layer and in the semiconductor layer below a part of the second layer, and to electrically connect the first base region of the second conduction type and the first body region of the second conduction type,

(B – 7) forming a source region of a first conduction type of the first field effect transistor at least in a part of a first region surrounded by the gate electrode layer, the first layer and the element isolation region,

(B – 8) forming a drain region of the first conduction type of the first field effect transistor in a part of a second region surrounded by the gate electrode layer, the second layer and the element isolation region,

(B – 9) forming a first collector region of the first conduction type of the first bi-polar transistor in a part of a second region surrounded by the first gate electrode layer, the second layer and the element isolation region,

(B – 10) forming a first emitter region of the first conduction type of the first bi-polar transistor in a third region surrounded by the first layer, the second layer and the element isolation region, and

(B – 11) electrically connecting the first body region of the second conduction type and the source region of the first conduction type;

the step (C) of forming a second field effect transistor and a second bi-polar transistor in the second element forming region,

wherein the step (C) comprises the steps of:

(C – 1) forming a first body region of the first conduction type in the semiconductor layer at least in a forming region where a second gate electrode layer is to be formed and a forming region where a fourth layer is to be formed,

(C – 2) forming a second body region of the second conduction type at least in a part of the semiconductor layer in a forming region where a third layer is to be formed,

(C – 3) forming a second gate electrode layer on the semiconductor layer in the second element forming region,

(C – 4) forming a third layer on the semiconductor layer in the second element forming region, wherein the third layer has one end section continuing to the second gate electrode layer or the fourth layer, and another end section reaching the element isolation region,

(C – 5) forming a fourth layer on the semiconductor layer in the second element forming region, wherein the fourth layer has one end section continuing to the second gate electrode layer or the third layer, and another end section reaching the element isolation region,

(C – 6) forming a second impurity diffusion layer of the second conduction type in the semiconductor layer in a sixth region surrounded by the third layer, the fourth layer and the element isolation region,

(C – 7) conducting a thermal treatment to thermally diffuse the second impurity diffusion layer of the second conduction type to form a second base region of the second conduction type of the second bi-polar transistor below a part of the third layer and in the semiconductor layer below a part of the fourth layer, and to electrically connect the second base region of the second conduction type and the second body region of the second conduction type,

(C – 8) forming a drain region of the second conduction type of the second field effect transistor in a fourth region surrounded by the second gate electrode layer, the third layer and the element isolation region,

and electrically connecting the drain region of the second conduction type to the second base region of the second conduction type through the second body region of the second conduction type.

(C – 9) forming a source region of the second conduction type of the second field effect transistor in a part of a fifth region surrounded by the second gate electrode layer, the fourth layer and the element isolation region.

(C – 10) forming a second collector region of the first conduction type of the second bi-polar transistor in a part of a fifth region surrounded by the second gate electrode layer, the fourth layer and the element isolation region,

and electrically connecting the second collector region of the first conduction type to the first body region of the first conduction type,

(C – 11) forming a second emitter region of the first conduction type of the second bi-polar transistor in a sixth region surrounded by the third layer, the fourth layer and the element isolation region, and

(C – 12) electrically connecting the source region of the second conduction type and the second collector region of the first conduction type;

the step (D) of electrically connecting the first collector region of the first conduction type and the second emitter region of the first conduction type; and

the step (E) of electrically connecting the first gate electrode layer and the second gate electrode layer.

18. A method for manufacturing a semiconductor device according to claim 17, further comprising the step of forming a third body region of the second conduction type in the semiconductor layer below the second layer in the first element forming region and in the semiconductor layer adjacent to the element isolation region.

19. A method for manufacturing a semiconductor device according to claim 18, further comprising the step of forming a fourth body region of the second conduction type in the semiconductor layer below the fourth layer in the second element forming region and in the semiconductor layer adjacent to the element isolation region.

20. A method for manufacturing a semiconductor device according to claim 17, wherein the first conduction type is n-type, and the second conduction type is p-type.

21. A method for manufacturing a semiconductor device according to claim 17, wherein the first conduction type is p-type, and the second conduction type is n-type.

22. A method for manufacturing a semiconductor device according to claim 17, wherein the semiconductor layer is a silicon layer.